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A DC-to-DC Converter With Constant Output Voltage

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ABSTRACT

A simple dc-to-dc inverter circuit has been developed which provides a constant average dc voltage output for wide ranges of input voltage. This circuit was designed to demonstrate the basic principles involved, and no attempt was made to maximize the efficiency, which undoubtedly could be improved considerably.

The basic requirements that must be incorporated in this circuit are (a) each half-cycle must be triggered at a constant frequency, (b) the time duration of each half-cycle must be less than the time between successive triggering half-cycles, (c) the power transistors must be cut off when the power core saturates, and (d) turn-off of one half-cycle must not spontaneously initiate the succeeding half-cycle.

An inverter circuit operating on these principles would provide a relatively simple method of providing a dc-to-dc converter having a constant voltage output, regardless of variations in input voltage or load, over relatively large ranges. Since it is based on switching techniques, its efficiency is high over its full operating range.

PROBLEM STATUS

This is a final report on one phase of the problem; work on other phases continues.

AUTHORIZATION

NRL Problem E01-05
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A DC-TO-DC CONVERTER WITH CONSTANT OUTPUT VOLTAGE

INTRODUCTION

In conventional static dc-to-dc converters the output voltage and operating frequency are directly proportional to the input voltage. Since the output is rectified, the change in operating frequency is unimportant, except insofar as it affects the efficiency. However, any practical device, subject to a wide range of input voltages or loads, must be provided with some type of voltage regulator. Such regulators can be classified as either dissipation or switching types. The dissipation types are very inefficient, because the excess power is being dissipated as heat. The switching types are more efficient, because the power is either on or off and the regulation is obtained by varying the ratio of the on-to-off time. The inverter described in this report is so constructed that this regulator switching function is an inherent feature of its design, and a constant average output is automatically achieved for all input voltages above the designed threshold voltage.

OPERATION OF CIRCUIT

The principle on which the inverter circuit is based depends on the fact that in a transformer having a square-loop magnetic core the secondary voltage amplitude is *directly* proportional to the input voltage, while the width of the pulse (time for the core to saturate) is *inversely* proportional to the input voltage. By triggering each half-cycle at a constant frequency and maintaining the output off after each half-cycle, the average value of voltage remains constant, provided the core saturates in less time than the triggering half-cycle.

The circuit diagram shown in Fig. 1 consists of two conventional transistorized static inverters, each of which provides a distinct function. The first inverter operates at a constant input voltage provided by a Zener diode dissipation-type regulator, and its output provides the constant-frequency triggering pulses for the main power inverter. The Zener diode regulator is inefficient for very high input voltages but was used in this circuit for simplicity.

The main power inverter is operated directly from the input voltage, and its core is designed to saturate in less time than one-half cycle of the trigger inverter. It is self-driven and therefore provides the cutoff feature required after saturation. The silicon controlled rectifiers in each base drive circuit prevent the spontaneous initiation of the succeeding half-cycle, when the preceding pulse is terminated by the core saturation. The starting pulse from the triggering inverter performs two distinct functions: it turns the appropriate silicon-controlled rectifier (SCR) on and it instantaneously turns on the main power transistor. The resulting instantaneous pulse through the power transistor and the primary winding induces a voltage in the base driving coil to maintain both the main power transistor and the associated base SCR in the conducting state. This condition is maintained and also produces the square-wave output pulse in the secondary winding, until the core saturates. When this happens, the base drive voltage and current drop to zero, and both the power transistor and its associated base SCR are turned off.

In a conventional static inverter this turnoff would initiate a pulse in the base circuit of the other transistor to spontaneously turn it on. However, in this circuit such a pulse is blocked by the SCR in the base circuit, which is turned off, and the initiation of the

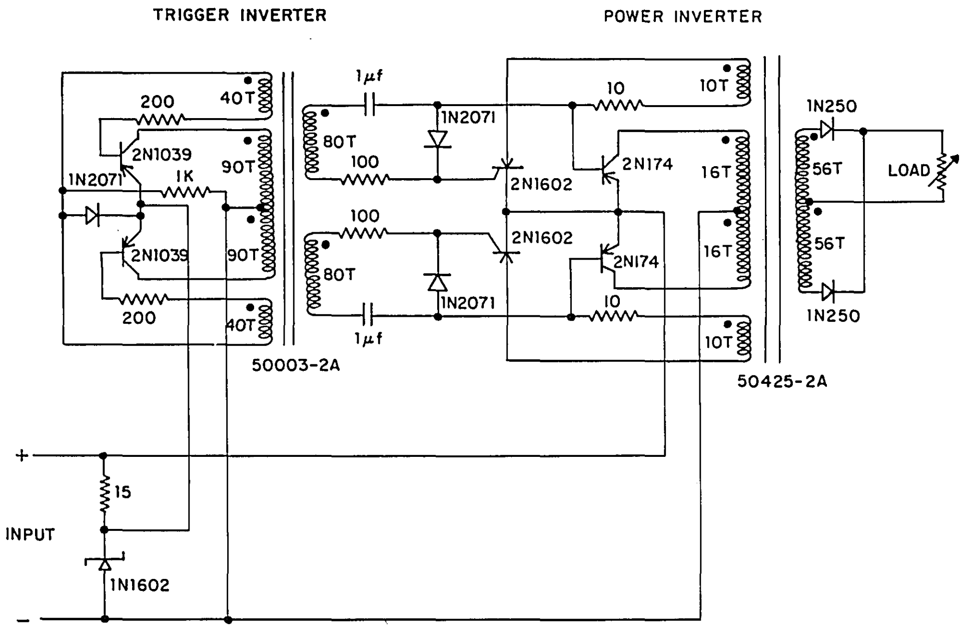

Fig. 1 - Circuit diagram of two conventional transistorized static inverters

succeeding half-cycle must await its own triggering pulse. Thus, the output voltage consists of a series of pulses, as shown in Figs. 2a, 2b, and 2c, all at no load and input voltages of 9, 12, and 15 volts, respectively. Each of these pulses has an amplitude directly proportional to the input voltage and a time duration inversely proportional to the input voltage and occurs at a constant frequency rate. These characteristics provide an *average* voltage output that is constant, regardless of the input voltage. Since this characteristic is obtained by switching action, the efficiency is maintained at a high level over a very wide operating range, limited only by the voltage limitations of its components and the ripple specifications for the output. The output wave shape is altered slightly by loading, as seen in Fig. 2d (12-volt input and 25-ohm load on output), but the output-voltage regulation characteristic is still maintained as can be seen from Table 1. The wave shapes shown in Fig. 2 are the inverter output wave shapes before rectification.

The data given in Table 1 show the constancy of the output voltage for a wide range of input voltages and various resistive loads. For a given load, an input-voltage change of 100% causes an output-voltage change of approximately 2-1/2%. The upper limit of input-voltage operation depends only on the maximum current and voltage limitations of the transistors used. This particular circuit was designed for operation at a frequency of approximately 1000 cycles/second and a lower threshold voltage of 9 volts. All voltages and currents were rectified and measured by means of D'Arsonval-type dc meters, which are incapable of following the 1000-cycle/second pulses and, therefore, served to average the parameters being measured.

The basic requirements that must be incorporated in this circuit are:

1. Each half-cycle must be triggered at a constant frequency.

2. The time duration of each half-cycle must be less than the time between successive triggering half-cycles.

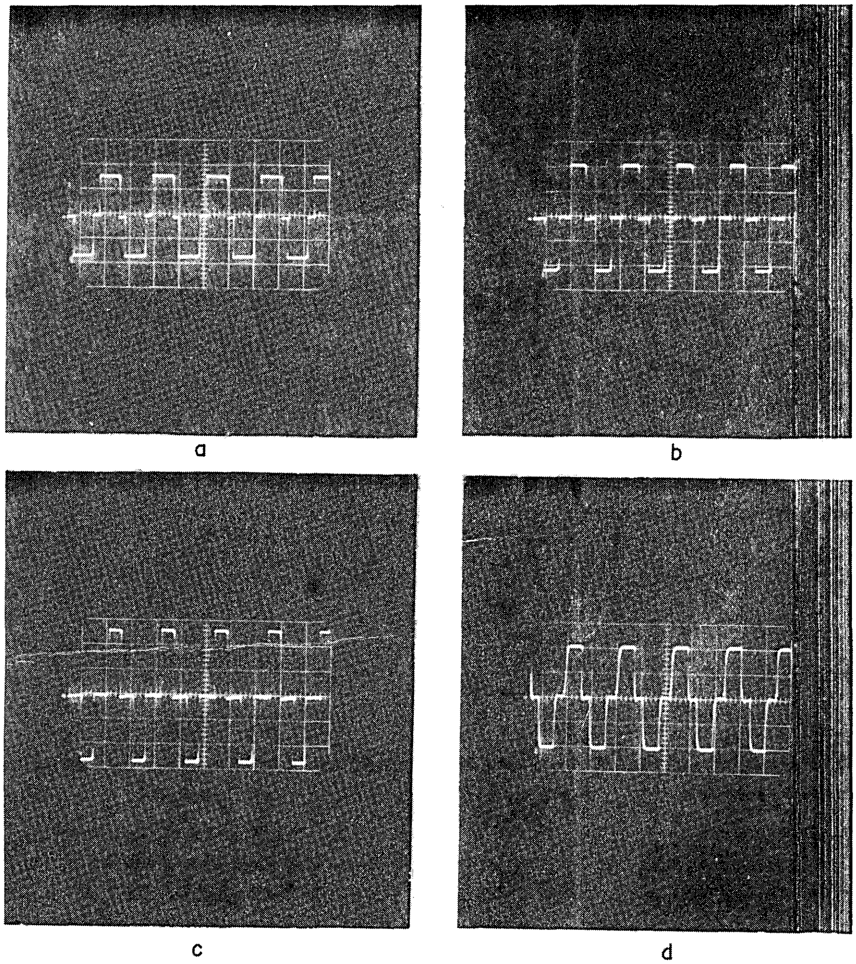

Fig. 2 - Inverter output wave-shapes before rectification. The horizontal scale represents 0.5 millisecond per division and the vertical scale represents 20 volts per division. (a) 9-volt input with no load, (b) 12-volt input with no load, (c) 15-volt input with no load, and (d) 12-volt input with a 25-ohm load.

3. The power transistors must be cut off when the power core saturates.

4. Turnoff of one half-cycle must not spontaneously initiate the succeeding half-cycle.

This circuit was designed to demonstrate the basic principles involved, and no attempt was made to maximize the efficiency, which undoubtedly could be improved considerably. The greatest loss occurs in the Zener diode regulator for the trigger inverter. If this loss is neglected, the efficiency is improved considerably and is maintained high throughout the entire operating range. A desirable change, if efficiency is important, would be to incorporate a more efficient input-voltage regulator than that provided by the Zener diode shown in Fig. 1. It was used in this case for simplicity.

Undoubtedly other switching circuits could be devised using these principles, but it is believed that the circuit shown in Fig. 1 is the simplest method of satisfying all of these requirements.

Table 1
Constant Output Voltage of a DC-to-DC Converter
(All currents and voltages are average measured values)

Input (volts)	Load (ohms)	Input to Power Inverter		Output to Load	
		Volts	Amperes	Volts	Amperes
9	–	6.45	0.70	23.7	–
12	–	6.55	0.75	23.9	–
15	–	6.67	0.80	24.2	–
18	–	6.80	0.89	24.3	–
9	50	6.48	2.58	23.4	0.48
12	50	6.58	2.70	23.7	0.48
15	50	6.70	2.86	23.8	0.49
18	50	6.80	3.20	24.0	0.49
9	25	6.51	4.25	23.3	0.97
12	25	6.60	4.44	23.4	0.97
15	25	6.65	4.65	23.6	0.98
18	25	6.67	5.00	23.7	0.98

RESULTS

An inverter circuit operating on the principles outlined above would provide a relatively simple method of providing a dc-to-dc converter having a constant voltage output, regardless of variations in input voltage or load, over relatively large ranges.

Since it is based on switching techniques, its efficiency is high over its full operating range.

It should have application in the medium power field, up to the current and voltage limitations of the power transistors used.

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